CLAIMS

1. An insulated gate field effect transistor, comprising:

a source region (14) of first conductivity type;

a body region (12) of second conductivity type opposite to the first conductivity type adjacent to the source region;

a drift region (10) of exclusively the first conductivity type adjacent to the body region;

a drain region (8) of first conductivity type adjacent to the drift region, so that body and drift regions are arranged between the source and drain regions, the drain region being of higher doping density than the drift region; and

insulated trenches (20) extending from the source region (14) through the body region (12) and into the drift region (10), each trench (20) having sidewalls (22), and including insulator (28) on the sidewalls, and a conductive gate electrode (32) between the insulating sidewall,

wherein the base of each trench (20) is filled with an insulator plug (30) adjacent to substantially all of the length of the drift region (10) between the body region (12) and drain region (8), and the respective gate electrode (32) is provided in the trench (20) over the plug (30) adjacent to the source and body regions (14,12).

2. An insulated gate field effect transistor according to claim 1 wherein the doping concentration in the drift region (10) is lower adjacent to the body region than adjacent to the drain region.

3. An insulated gate field effect transistor according to any preceding claim wherein the doping concentration in the body region (12) is in the range 0.5 to 3x 10^{17} cm^{-3}, and the doping concentration in the drift region (10) is in the range 10^{15} to 2x10^{17} cm^{-3}.

4. An insulated gate field effect transistor according to any preceding claim wherein the plug (30) is of dielectric filler filling the trench

between the insulator (28) on the sidewalls (22) adjacent to the drain region (10).

5. An insulated gate field effect transistor according to any preceding claim having a semiconductor body (2) having opposed first (4) and second major surfaces (6),

wherein the source region (14) is at the first major surface over the body region (12), the body region (12) is over the drift region (10) and the drift region (10) is over the drain region (8), and

the trench extends from the first major surface towards the second major surface through the source (14), body (12) and drift (10) regions.

6. An insulated gate field effect transistor according to claim 5 having a plurality of cells (40), each cell having a source region (16) at the centre of the cell surrounded by the insulated trench (20).

7. An insulated gate field effect transistor according to claim 6 wherein the cells (40) have a hexagonal geometry.

8. An insulated gate field effect transistor according to claim 6 or 7 wherein the trench (20) has gate oxide (28) on the sidewalls, and the base (24) of the trench adjacent to the drift region (10) is filled with filler oxide (30) between the gate oxide (24) on the sidewalls (22) on either side of the trench.

9. An insulated gate field effect transistor according to claim 5 having a plurality of cells (40), arranged as stripes across the first major surface (4) with alternating trenches (20) and source regions (14).

10. An insulated gate field effect transistor according to any of claims 6 to 10 wherein the cell pitch is in the range 0.2 to 0.7 micron.